COA COMPREHENSIVE VIVA QUESTIONS – GROUP 5

1)Memory interleaving is done to:

a) Increase the amount of logical memory

b) Reduce memory access time

c) Simplify memory interfacing

d) Reduce page faults

Answer: b) Reduce memory access time

2)Consider the following sequence of micro-operations:

MBR ← PC

MAR ← X

PC ← Y

Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

a) Instruction fetch

b) Operand fetch

c) Conditional branch

d) Initiation of interrupt service

Answer: d) Initiation of interrupt service

3)In a virtual memory system, the size of the virtual address is 32-bit, the size of the physical address is 30-bit, the page size is 4 Kbytes, and the size of each page table entry is 32-bit. The main memory is byte addressable. What is the maximum number of bits that can be used for storing protection and other information in each page table entry?

A) 2

b) 10

c) 12

d) 14

Answer: d) 14

4)Memory Buffer Register (MBR) is connected to:

a) Control Bus

b) Address Bus

c) Data Bus

d) System Bus

Answer: c) Data Bus

5)Which of these memories would have the lowest access time in a system?

a) Main Memory

b) Magnetic Disk

c) Registers

d) Cache

Answer: c) Registers

6)A 5-stage pipeline has a clock cycle time of 10 ns. If the pipeline is operated at a frequency of 100 MHz, what is the total time taken to execute 100 instructions?

A) 500 ns

b) 1000 ns

c) 5000 ns

d) 10000 ns

Answer: c) 5000 ns

7)The search concept used in associative memory is:

a) Parallel search

b) Sequential search

c) Binary search

d) Selection search

Answer: a) Parallel search

8)Match the following address modes with their corresponding applications:

(a) Immediate address mode

(b) Direct address mode

(c)Indirect address mode

(d) Index addressing mode

(e)Base address mode

(f) Relative address mode

(1) Local variables

(2) Relocatable programs

(3) Pointer

(4) Locality of reference

(5) Arrays

(6) Constant Operands

Options:

a) a-6, b-1, c-3, d-5, e-2, f-4

b) a-5, b-4, c-6, d-3, e-1, f-2

c) a-3, b-5, c-2, d-4, e-1, f-2

d) a-6, b-5, c-2, d-3, e-1, f-4

Answer: a) a-6, b-1, c-3, d-5, e-2, f-4

9)Consider a system that uses a DMA controller to transfer data between a device and memory. If the DMA controller can transfer 4 bytes of data in a single cycle, what is the maximum data transfer rate?

A) 16 bytes/cycle

b) 32 bytes/cycle

c) 64 bytes/cycle

d) 128 bytes/cycle

Answer: a) 16 bytes/cycle

10)The basic component of an arithmetic circuit is:

a) Parallel subtractor

b) Parallel adder

c) Half adder

d) Full adder

Answer: b) Parallel adder

11)Which of the following I/O techniques is used to transfer data between a device and memory without CPU intervention?

A) Programmed I/O

b) Interrupt-driven I/O

c) Direct Memory Access (DMA)

d) All of the above

Answer: c) Direct Memory Access (DMA)

12)The main advantage of using a single-bus structure is:

a) Fast data transfers

b) Cost-effective connectivity and speed

c) Cost-effective connectivity and ease of attaching peripheral devices

d) None of the mentioned

Answer: c) Cost-effective connectivity and ease of attaching peripheral devices

13)Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O bandwidth?

A) Transparent DMA and Polling interrupts

b) Cycle-Stealing and Vectored interrupts

c) Block Transfer and Vectored interrupts

d) Block Transfer and Polling interrupts

Answer: c) Block Transfer and Vectored interrupts